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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,184	12/10/2001	Jeroen Anton Johan Leijten	NL 000681	1259

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,184	LEIJTEN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/16/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RD

1. Claims 1-11 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al (WO 00/33178) in view of (4,975,836) in view of Dictionary of IEEE, 2000, 7th Edition, page 494.

3. As to claim 1 , Tremblay et al discloses a signal processing device comprising at least :

a) plurality of functional units (UCI-UCn) (figure 5A, elements 520-526,* figure 6, elements 620-626) for processing digital data based on an instruction word (figure 5C),

b) respective ones of said functional units, (For several reasons the Examiner asserts that a plurality of register files is disclosed. First, the claim language and a plurality of register files (RFI-RFn) for storing results obtained from simply states $'a plurality of register files" but gives no indication of these being physically separate register files. The register segments of page 7, lines 18-25 include three "virtual register files" that contain replicated data for speed and area considerations. Second, figure 2 elements 224 and figure 5A elements 510-516, for example, both clearly show that the register segments may be separate

register files. Third, the included IEEE standard definition of "register file" states that a register file is data set of registers which may be addressed by their number in the set". Therefore, each of the replicated register segments or sets, which each have their own ports and are thus separately addressable (as given above and in figures 2 and 5A, for example), are in fact register files.), wherein said functional units are arranged to write a result to a predetermined register of said register files by using a register address (RRI) derived from said instruction word; (Figures 5A and 6 show that results are written to the register files via the line that returns to the register files from the functional units. Figure 5C along with page 12, lines 6-15 show that the instruction word specifies registers to use in the different register files (segments) using a certain number of bits, or an address (as described in the next paragraph of the reference), and register allocation means (RA) for selecting at least two of said register files (RFI-RFn) and for supplying said register address to said selected register files, if said instruction word comprises a corresponding indication. (Figure 3 and 5A and page 9, lines 25-30 show that the split register file (multiple register files) holds all the operands for instructions. The figure as well as the section of page 7 (replication) show that broadcast writes are performed to each register file and thus they are all selected for this write. As shown above, the instruction provides indication showing the register address to write to, which then corresponds to the broadcast write of multiple register files. The structure for this means is shown in the figures, where the register files receive the data and inherently the register index for this write to all of the register files, and thus

is consistent with the structure given in the specification.

4. The included IEEE publication is used to show the definition of a register file. The standard definition of "register file" states that a register file is "a set of registers which may be addressed by their number in the ser. Therefore, each of the replicated register segments or sets, which each have their own port and are thus separately addressable (as given above and in figures 2 and 5A, for example), are in fact register files.

5. Tremblay is used as primary reference because it shows clearly the structure of respective functional units (see fig.600). Hirosawa is used to supplement the teaching of register file selection.

6. Tremblay et al (WO 00/33178) and Dictionary of IEEE, 2000, 7th Edition, page 494 were cited to applicant on the record , therefore copies are not being provided herein .

7. Tremblay did not specifically show the selection of the register files as clamed. However, Hirosawa disclosed a system including a selection of among register files (see selection of register groups [38] in fig.6, see also fig.7, col.9, lines 29-68, col.10, lines 1-55). It would have been obvious to one of ordinary skill in the art to use Hirosawa in Tremblay for including the selection of register files as claimed because the use of Hirosawa could provide Tremblay the ability to designate a predefine set of registers based on a given system conditions, and therefore , increasing the adaptability of the storage access control in Tremblay, and it could be done by configuring the selection

circuit of Hirosawa into Tremblay with modified control parameter (e.g. the R/W ports) so that the specific selection of the register files of Hirosawa could be recognized by Tremblay, and because Tremblay also taught that his local register were addressed in a local register range outside the global register range (see abstract), which was an indication of the need of the selection of a specific register group to accept address range outside the global range in order to provide enhanced flexibility of the storage control, and in doing so, provided a motivation.

8. As to claim 2, limitations of claim 1 will not be repeated herein. Tremblay disclosed wherein said functional units (UCI-UCn) are arranged to supply said corresponding indication to said register allocation means (RA). Since the indication is the register address, the RA must receive the indication so the address of the broadcast write is known.)

9. As to claim 3, Tremblay et al discloses said signal processing device is a programmable VLIW processor (abstract), and said register files are partitioned register files (RF1-RFn), wherein a data stationary instruction encoding is used. As shown above, the register file is split into 4 separate or partitioned register files. (see Figure 5C shows a data stationary instruction encoding where the encoding of the instruction is stationary such that the encoding is fixed so that certain bits of data are always at certain lodations in the word.)

10. As to claim 4, Tremblay et al discloses the device according to claim 1, wherein said corresponding indication is an information stating that said result is to be

written to said register address of said selected register files (as shown above).

11. As to claim 5, Tremblay disclosed the corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files. As shown above, the indication is an address or index to a broadcast register that is written to. Since this broadcast register is written to, the data to be written is inherently the result of some operation from a functional unit.)

12. As to claim 6, Tremblay disclosed the register allocation means comprises demultiplexing means (DMI-DM3) for demultiplexing said result and said register address (RRI) to said selected register files . in response to said corresponding indication. (As shown above, the register files receive a register address to write to and a result for writing to the address. Page 14, lines 22-23 show that the write ports of the register files receive data from the functional units including the result and the address or indicator. Page 15, lines 9-1 1 show that the write ports (for writing the result) comprise word lines for addressing a cell or register (also shown in page 14, lines 27-28) and bit lines for carrying the data (result).

13. Thus the write port, which contains the result and address data, is demultiplexed into separate word and bit lines that contain the address and result, respectively

14. As to claim 7, Tremblay disclosed the functional units are functional unit clusters (UC1-UCn). Figures 5A and 6 show the functional units and that these units are grouped into a cluster. Another interpretation, would be to divide the functional units into

two clusters, one cluster comprising elements 520 and 522 (or 620 and 622) and another cluster comprising elements 524 and 526 (or 624 and 626) and thus we have multiple functional unit clusters.)

15. As to claim 8, Tremblay et al discloses a method of supplying a signal processing result to a plurality of registers arranged in different register files (RA1-RAn) of a signal processing device (figure 5A, elements RFO-RF3,' figure 6, elements 610-616), said method comprising the steps of:

a) determining a register address (RRI) based on an instruction word; (Figure 5C along with page 12, lines 6-15 show that the instruction word specifies registers to use in the different register files (segments) using a certain number of bits, or an address (as described in the next paragraph of the reference.)

b) supplying said register address to said plurality of register files, The register address of above is inherently given to the register files so that the appropriate register is selected.), and selecting said plurality of register files based on a corresponding indication in said instruction word and supplying said register address to said selected register files. (see Figure 3 and page 9, lines 25-30 show that the split register file (multiple register files) holds all the operands for instructions). The figure shows that broadcast writes are performed to each register file and thus they are all selected for this write. As shown above, the instruction provides indication showing the register address to write to, which then corresponds to the broadcast write of multiple register files.)

16. As to claim 9, Tremblay et al disclosed the corresponding indication is an information stating that said result is to be written to said register address of said selected register files (as shown above).

17. As regard to claim 10, Tremblay et al discloses the method according to claim 8, wherein said corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files (as shown above).

18. As to claim 11, Tremblay et al discloses the method according to anyone of claim 8, wherein said selection step comprises a demultiplexing step of : demultiplexing said result and said register address to said selected register files in response to said corresponding indication. (As shown above, the register files receive a register address to write to and a result for writing to the address. Page 14, lines 22-23 show that the write ports of the register files receive data from the functional units including the result and the address or indicator. (see Page 15, lines 9-11 show that the write ports for writing the result comprise word lines for addressing a cell or register (also shown in page 14, lines 27-28)) and bit lines for carrying the data (result). Thus the write port, which contains the result and address data, is demultiplexed into separate word and bit lines that contain the address and result, respectively.)

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Agrawal et al. (5,958,038) is cited for the background teaching of the plurality of register files with a selection circuit (see fig.2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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